CODE EEL204	DIGITAL ELECTRONICS LAB	CATEGORY	L	T	P	CREDIT
		PCC	0	0	3	2

Course Outcomes : After the completion of the course the student will be able to:

CO 1	Formulate digital functionsusing Boolean Algebra and verify experimentally.
CO 2	Design and implement combinational logic circuits.
CO 3	Design and implement sequential logic circuits.
CO 4	Design and fabricate a digital circuit using the knowledge acquired from the laboratory.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	1	1	3	3			2	3	3		1
CO 2	3	3	3	3	3			2	3	3		1
CO 3	3	3	3	3	3			2	3	3		1
CO 4	3	2	1	3	2			2	3	3	2	3

LIST OF EXPERIMENTS

Pre-lab assignment :Familiarisation of Logic Gates, Identification of typical logic ICs, Interpreting IC datasheets.

1. Verification & Realisation of De Morgan's theorem.
2. Realisation of SOP & POS functions after K-map reduction.
3. Half adder & Full adder using gates.
4. 4-bit adder/subtractor & BCD adder using IC 7483.
5. Realisation of 2-bit comparator using gates and study of four-bit comparator IC 7485.
6. BCD to decimal decoder and BCD to 7-segment decoder & display.
7. Study of multiplexer IC and realization of combinational circuits using multiplexers.
8. Realization of RS, T, D & JK flip flops using gates.
9. Study of flip flop ICs (7474 & 7476).
10. Realisation of ripple up and down counters and modulo-N counter using flip-flops.
11. Study of counter ICs (7490, 7493).
12. Design of synchronous up, down & modulo-N counters.
13. Realization of 4-bit serial IN serial OUT registers using flip flops.
14. Study of shift register IC 7495, ring counter and Johnsons counter.
15. VHDL implementation of full adder, 4 bit magnitude comparator

Course Project : Students have to do a mandatory course project (group size not more than 4 students) using digital ICs or Programmable Logic Devices (CPLD/FPGA) to realise a functional digital circuit. A maximum of 5 marks shall be awarded for this project (to be evaluated along with the final internal test).

Example of course projects :

1. Realisation of a real-time digital clock with display.
2. Digital Alarms
3. ALU (May be implemented in FPGA)
4. Digital Security Monitoring System
5. Traffic Control

Assessment Pattern :

Mark distribution :

Total Marks	CIE	ESE	ESE Duration
150	75	75	2.5 hours

Continuous Internal Evaluation (CIE) Pattern:

Attendance	Regular Lab work	InternalTest	CourseProject	Total
15	30	25	5	75

End Semester Examination Pattern:

The following guidelines should be followed regarding award of marks:

(a) Preliminary work : 15 Marks
(b) Implementing the work/Conducting the experiment : 10 Marks
(c) Performance, result and inference (usage of equipment and troubleshooting) : 25 Marks
(d) Viva voce : 20 marks
(e) Record : 5 Marks

General instructions : Practical examination to be conducted immediately after the second series test covering entire syllabus given below. Evaluation is a serious process that is to be conducted under the equal responsibility of both the internal and external examiners. The number of candidates evaluated per day should not exceed 20. Students shall be allowed for the University examination only on submitting the duly certified record. The external examiner shall endorse the record.

Reference Books:

1. Floyd T.L, Digital Fundamentals, 10/e, Pearson Education, 2011.
2. C.H.Roth and L.L.Kimney Fundamentals of Logic Design, 7/e, Cengage Learning, 2013.