EE365Prerequisite: NCourse Object:To impleTo impleSyllabusCombinationalSequential DesVHDL SimulatiExpected outsAfter completii. Desiii. Impliii. Progiv. HardText Book:Mark ZvEducationReferences:1. A Anano2. John F V3. Morris NModuleIntroConConI conI conIntroJohn F V3. Morris NIntro<	Digital System Design           Nil           tives           ble designing and building of real digital circuits           lement VHDL programming in digital system design           logic using VHDL gate models, Combinational           sign, VHDL Models of Sequential Logic Blocks,           tion, VHDL Synthesis, Testing Digital Systems, Des           come.           ing the course, the students will be able to           ign any Digital Circuit for practical application           element any digital system using VHDL           gram any VHDL code for practical implementation           dware realization of any complex VHDL system.	building blocomplex S ign for Testa	earson	6 chronous Systems,			
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2. John F V 3. Morris M Module Intro Prog I Con Con Con Arch Sign benc	dakumar, Digital Electronics Prentice Hall India Feb	2009					
3. Morris N Module Intro Prog I Com Com Arch Sign benc	Wakerly Digital Design Pearson Education Delhi	2002					
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IV	<ul> <li>VHDL Models of Sequential Logic Blocks : Latches , Flip-Flops , J K and T Flip Flop , Registers and Shift Registers ,Counters , Memory, Sequential Multiplier, Test benches for Sequential Building Blocks</li> <li>Complex Sequential Systems : Data path / Control Partitioning ,Instructions, A Simple Microprocessor, VHDL model of a Simple Microprocessor</li> </ul>	8	15%		
SECOND INTERNAL EXAMINATION					
V	<ul> <li>VHDL Simulation: Event Driven Simulation, Simulation of</li> <li>VHDL models, Simulation modelling issues, Fire Operations.</li> <li>VHDL Synthesis: RTL Synthesis, Constraints, Synthesis for</li> <li>FPGAs, Behavioural Synthesis, Verifying Synthesis Results</li> </ul>	8	20%		
VI	Testing Digital Systems : Need for Testing , Fault Models , Fault oriented Test Pattern Generation , Fault Simulation, Fault Simulation in VHDL Design for Testability : Ad Hoc Testability improvements , Structured Design for Test , Built-in-Self-Test , Boundary scan ( IEEE 1149 .1 )	7	20%		
END SEMESTER EXAM					

**QUESTION PAPER PATTERN:** 

Maximum Marks: 100

Exam Duration: 3Hourrs.

Part A: 8 compulsory questions.

One question from each module of Module I - IV; and two each from Module V & VI.

Student has to answer all questions. (8 x5)=40

**Part B**: 3 questions uniformly covering Modules I & II. Student has to answer any 2 from the 3 questions:  $(2 \times 10) = 20$ . Each question can have maximum of 4 sub questions (a,b,c,d), if needed.

Estd.

**Part C**: 3 questions uniformly covering Modules III & IV. Student has to answer any 2 from the 3 questions:  $(2 \times 10) = 20$ . Each question can have maximum of 4 sub questions (a,b,c,d), if needed.

**Part D**: 3 questions uniformly covering Modules V & VI. Student has to answer any 2 from the 3 questions:  $(2 \times 10) = 20$ . Each question can have maximum of 4 sub questions (a,b,c,d), if needed.